

## **What is claimed is:**

**[Claim 1]** A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

- forming an opening for semiconductor structure in a dielectric layer on a substrate;
- depositing a sacrificial layer over the opening;
- performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall on the opening;
- depositing a conductive liner over the opening;
- depositing a metal in the opening;
- planarizing the metal and the conductive liner;
- removing the sacrificial layer sidewall to form a void; and
- depositing a cap layer over the void to form the gas dielectric structure.

**[Claim 2]**

The method of claim 1, wherein the opening includes at least one wiring line opening and at least one via.

**[Claim 3]** The method of claim 2, wherein the void extends along a side of the at least one via.

**[Claim 4]** The method of claim 1, wherein the forming step includes performing a dual damascene process.

**[Claim 5]** The method of claim 1, wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask.

**[Claim 6]** The method of claim 1, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer.

**[Claim 7]** The method of claim 1, wherein the conductive liner includes at least one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb).

**[Claim 8]** The method of claim 1, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al), silicon dioxide (SiO<sub>2</sub>) and titanium (Ti).

**[Claim 9]** The method of claim 1, wherein the removing step includes etching the sacrificial sidewall layer using one of: a) water (H<sub>2</sub>O) and sodium hydroxide (NaOH); b) water (H<sub>2</sub>O) and hydrofluoric acid (HF); and c) hydrofluoric acid (HF) and hydrochloric acid (HCl).

**[Claim 10]** The method of claim 9, wherein in the case that water (H<sub>2</sub>O) and sodium hydroxide (NaOH) are used as an etchant, the ratio of H<sub>2</sub>O to NaOH is no greater than approximately 10:1 and no less than 1:1.

**[Claim 11]** A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

- performing a dual damascene process to form an opening including at least one wiring opening and at least one via in a dielectric layer on a substrate;
- depositing a sacrificial layer over the opening;
- performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall;
- depositing a conductive liner over the opening;
- depositing a metal in the opening;
- planarizing the metal and the conductive liner;
- removing the sacrificial layer sidewall to form a void; and
- depositing a cap layer over the void to form the gas dielectric structure.

**[Claim 12]** The method of claim 11, wherein the void extends along a side of the at least one via.

**[Claim 13]** The method of claim 11, wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask.

**[Claim 14]** The method of claim 11, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride ( $\text{Si}_3\text{N}_4$ ) and silicon dioxide ( $\text{SiO}_2$ ).

**[Claim 15]** The method of claim 11, wherein the conductive liner includes at least one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb).

**[Claim 16]** The method of claim 11, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al), silicon dioxide ( $\text{SiO}_2$ ) and titanium (Ti).

**[Claim 17]** A method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

- performing a via-first dual damascene process to form an opening including at least one wiring opening and at least one via in a dielectric layer on a substrate;
- depositing a sacrificial layer over the opening;
- performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall;
- depositing a conductive liner over the opening;
- depositing a metal in the opening;
- planarizing the metal and the conductive liner;
- removing the sacrificial layer sidewall to form a void that extends along a side of the at least one via; and
- depositing a cap layer over the void to form the gas dielectric structure.

**[Claim 18]** The method of claim 17, further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride ( $\text{Si}_3\text{N}_4$ ) and silicon dioxide ( $\text{SiO}_2$ ).

**[Claim 19]** The method of claim 17, wherein the conductive liner includes one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb).

**[Claim 20]** The method of claim 17, wherein the sacrificial layer includes one of the group consisting of: aluminum (Al), silicon oxide (SiO<sub>2</sub>) and titanium (Ti).